REMARKS

Claims 1, 3-4, 6-12, and 14-30 are pending in the application. No claims have been amended.

Claims 1, 3-4, 6-12, and 14-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Watkins et al, U.S. Patent No. 5,937,436 (hereinafter "Watkins") in view of Horstmann et al, U.S. Patent No. 6,125,433 (hereinafter "Horstmann") in view of Futral et al, U.S. Patent No. 6,112,263 (hereinafter "Futral") and further in view of Garcia et al., U.S. Patent No. 6,163,834 (hereinafter "Garcia").

Claim Rejections Under 35 U.S.C. §103(a)

Each of the pending claims have been rejected based on a combination of Watkins, Horstmann, Futral, and Garcia. Futral, however, is not a proper reference for a § 103(a) rejection. Futral is a "§ 102(e)-type" reference in that it was filed prior to the filing date of the present application (December 17, 1999) but issued afterwards (August 29, 2000). Both Futral and the present application have been assigned to Intel Corporation, and for all relevant points in time, the Applicant in Futral and the Applicants in the present application were under an obligation to assign their rights (or did assign their rights) in their respective applications to Intel Corporation. Under 35 U.S.C. § 103(c), Futral does not qualify as prior art to the presently claimed invention. In the current Office Action, the Examiner admits that features of each of the independent claims (i.e., claims 1, 9, 16, 21, and 26) are missing from the Watkins and Horstmann references. As detailed below features of the independent claims are missing from the newly-cited Garcia patent.

According to its abstracts, Horstmann discloses an optimized translation lookaside buffer (TLB) utilizes a least-recently-used algorithm for determining the replacement of virtual-to-physical memory translation entries; and Watkins discloses a network interface circuit including an address translation unit and a flush check circuit, and a method for checking for an invalid address translation within of the address translation unit.

Applicants contend that Horstmann, Watkins, and any combination thereof fail to teach or suggest each of said TPT entries including protection attributes to control read and write access to a given memory region of a host memory and a memory protection tag to specify whether said apparatus has permission to access said host memory, as recited in the independent claims.

Garcia fails to make up for the deficiencies of Watkins and Horstmann. Garcia refers to a two level transalation and memory registration system and method. As with Watkins and Hostmann, Garcia does not describe a host and ahost-fabric adapter as described in the pending claims. Since features of each of the pending claims are not taught or suggested by the cited references, reconsideration and withdrawal of the rejection of claims 1, 3-4, 6-12, and 14-30 under 35 U.S.C. §103(a) is respectfully requested.

Conclusion

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON

Dated: August 30, 2004

By: _____

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